



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/928,570 | 08/13/2001 | Rongxiang Hu | 01-099 | 7873 |

7590 10/22/2003

Sandeep Jaggi
Intellectual Property Law Department
LSI Logic Corporation
1551 McCarthy Boulevard, M/S D-106
Milpitas, CA 95035

| |
|----------|
| EXAMINER |
|----------|

UMEZ ERONINI, LYNETTE T

| | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

1765

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/928,570

Applicant(s)

HU ET AL.

Examiner

Lynette T. Umez-Eronini

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-11 is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The amendment filed 7/22/03 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: “. . . a semiconductor wafer which also has an exposed low dielectric constant material layer adjacent to the silicon carbide layer . . .”

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. “. . . a semiconductor wafer which also has an exposed low dielectric constant material layer adjacent to the silicon carbide layer . . .” is not described in the Specification nor depicted in the Drawing to best described the configuration of the semiconductor. The Specification discloses, “in particular, in the

Art Unit: 1765

example shown, one or more silicon carbide (SiC) films, or layers, 104, 106, and 108 are deposited above the substrate 103. Also, in this example, one or more low k (dielectric constant type material films 110 and 112 (e.g. silicon oxide, organo-silica-glass "OSG," etc.) are deposited between the SiC films 104, 106, and 108, as shown. Additionally, an underlying metal layer 114, such as copper (Cu), may be deposited under the first SiC film 104 and over various other layers 116 or structures formed in or deposited on the substrate 102" (page 2, lines, 22-28). The aforementioned fails to disclose an exposed low dielectric constant material layer adjacent to the silicon carbide layer.

Claim Objections

4. Claim 1 is objected to because of the following informalities: "carbon-tetrafluoritde" should read --carbon tetrafluoride--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

Art Unit: 1765

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow et al. (US 6,251,770 B1) and further in view of Chooi et al. (US 6,284,657 B1).

As pertaining to claim 1, Uglow teaches in the Description of the Related Art, "Semiconductor devices are made from multi-layer structures that are fabricated on semiconductor wafers" (column 1, lines 12-13). "As shown, a dielectric **10** is shown having a copper trench line **12** with a liner barrier **14**. A barrier layer **16a** is used to prevent copper from diffusing into the dielectric **10**. A first oxide layer **18a** is deposited over the barrier layer **16a**, and a trench stopping layer **16b** is deposited over the first oxide layer **18a**. A second oxide layer **18b** is then deposited over the trench stopping layer **16b**. In cases where the first and second oxide layers **18a** and **18b** are un-doped TEOS oxides or fluorine doped oxides, there are well developed etching techniques that provide excellent selectivities to the layers **16a** and **16b** . . . On the other hand, when lower dielectrics such as C-oxide are implemented for oxide layers **18a** and **18b**, the selectivity to the barrier layers **16** is reduced to ranges nearing about 5:1. This reduction in selectivity therefore causes the barrier layer **16a** to be removed at location

Art Unit: 1765

30, thereby exposing the underlying copper line **12** to oxygen" (column 1, line 47 – column 2, line 4). The above reads on,

A method of removing an exposed silicon carbide layer from an underlying layer during fabrication of an integrated circuit chip on a semiconductor wafer which also has an exposed low dielectric constant material layer adjacent to the silicon carbide layer, the method comprising:

flowing an etch chemical into contact with the silicon carbide layer and the low dielectric constant material; and

etching the exposed silicon carbide layer from the underlying copper layer without removing the exposed low dielectric constant material, **in claim 1**.

Ugnow differs in failing to teach the etch chemical selected from the group consisting of CF_4 , CHF_3 , CH_2F_2 , and CH_4 ; introducing a selectivity enhancing chemical into the flow of the etch chemical to create a combination flow of the etch chemical and the selectivity enhancing chemical; the selectivity enhancing chemical selected from the group consisting of H_2 and NH_3 , the selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material; and the combination flow without substantially removing the exposed low dielectric constant material, **in claim 1**;

introducing a selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into contact with the surface of the semiconductor wafer, **as in claim 3**; and

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into contact with the surface of the semiconductor, **as in claim 4**.

Swanson teaches, "Methods for removing SiC are known in the art. The following are some exemplary methods for removing portion 118 of SiC masking layer 104 . . . [. . . Removal rate for SiC relative to SiO₂ of 10:1 has been achieved.] using a chamber pressure: about 300 mTorr (gas flow 10-50 sccm) and RF Power density about 0.5-1 W/cm² (13.56 MHz); (2) CF₄ /O₂ /H₂, . . ." (column 4, lines 25-43). The aforementioned reads on,

introducing a selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into contact with the surface of the semiconductor wafer, **in claim 3**; and

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into contact with the surface of the semiconductor, **in claim 4**; and

the etch chemical selected is from the group consisting of CF₄, CHF₃, CH₂F₂, and CH₄; and the selectivity enhancing chemical selected from the group consisting of H₂ and NH₃, **in claim 1**. Since Swanson teaches etching the same layers with the same etchants as those of the claimed invention, then using Swanson's etchant in the same manner as that of the claimed invention would result the same in introducing a selectivity enhancing chemical into the flow of the etch chemical to create a combination flow of the etch chemical and the selectively enhancing chemical, the

Art Unit: 1765

selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material; and the combination flow without substantially removing the exposed low dielectric constant material, as in the claimed invention.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Uglow by using a well known method of removing silicon carbide layer as taught by Swanson for the purpose of achieving the best selectivity of silicon carbide with respect to a low dielectric constant material with a reasonable expectation of success.

8. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow (US '770 B1) in view of Swanson (US '590) as applied to claim 1 above, and further in view of Conboy et al. (US 5,904,487) and Bhardwaj et al. (US 6,0541,503).

Uglow in view of Swanson differ in failing to specify the selectivity enhancing chemical in a C:H:F ratio of about 1:1:2 to about 1:8:4, **in claim 2** and a temperature range of about -30 to about 80°C, and a power level in a range of about 200 to about 1500 watts, **in claim 5**.

Conboy teaches "Etch rate across the wafer can vary with variation of one or more process parameter including . . . process parameters associated with the plasma including pressure, temperature, composition, flow rate, etc. . . and process parameters associated with the wafer such as temperature" (column 2, lines 12-17) and Bhardwaj teaches the following parameters: . . . chamber pressure, plasma power . . . vary with

Art Unit: 1765

time (Abstract). Hence, Conboy and Bhardwaj provide evidence that variation in plasma composition (etchant ratio), substrate temperature, chamber pressure and plasma power are so-called "result effective variables."

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Uglow in view of Swanson by varying the plasma composition, pressure, and power and substrate temperature as taught by Conboy and Bhardwaj since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 717 F.2d 272, 205 USPQ 215 (CCPA 1980).

9. Claims 6, 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow et al. (US 6,251,770 B1) as applied to claim 1 above, and further in view of Swanson (US '590).

As pertaining to claim 6, Uglow teaches in the Description of the Related Art, "Semiconductor devices are made from multi-layer structures that are fabricated on semiconductor wafers. . . . In dual-damascene applications, the metallization interconnect lines are defined in trenches that are etched into dielectric layers. Typically, the interconnect metallization is a copper (Cu) material, and the conductive vias are also integrally formed of Cu" (column 1, lines 12-20). "As shown, a dielectric **10** is shown having a copper trench line **12** with a liner barrier **14**. A barrier layer **16a** is used to prevent copper from diffusing into the dielectric **10**. A first oxide layer **18a** is deposited over the barrier layer **16a**, and a trench stopping layer **16b** is deposited over the first

Art Unit: 1765

oxide layer **18a**. A second oxide layer **18b** is then deposited over the trench stopping layer **16b**. In cases where the first and second oxide layers **18a** and **18b** are un-doped TEOS oxides or fluorine doped oxides, there are well developed etching techniques that provide excellent selectivities to the layers **16a** and **16b**. . . . On the other hand, when lower dielectrics such as C-oxide are implemented for oxide layers **18a** and **18b**, the selectivity to the barrier layers **16** is reduced to ranges nearing about 5:1. This reduction in selectivity therefore causes the barrier layer **16a** to be removed at location 30, thereby exposing the underlying copper line **12** to oxygen" (column 1, line 47 – column 2, line 4). The above reads on,

A method for performing a damascene metallization process during fabrication of an integrated circuit chip on a semiconductor wafer comprising:

forming a copper layer on the semiconductor wafer;

forming a silicon carbide layer on the copper layer;

forming a layer of a low dielectric constant material on the semiconductor wafer;

removing a region of the low dielectric constant material to expose a portion of the silicon carbide layer and a portion of the low dielectric constant material;

flowing an etch chemical into contact with the silicon carbide layer and the low dielectric constant material; and

removing a region of the exposed silicon carbide layer, in claim 6. Uglow further teaches, "Obviously, if copper material were to were to be deposited into the inter-meta; dielectric, a device may fail to optimally perform in accordance with desired performance specifications" (column 2, lines 13-15), which suggests forming a metal

Art Unit: 1765

region into the removed regions of the low dielectric constant material and the silicon carbide layer, **in claim 6**; and forming the metal region by depositing copper (Cu) into the removed regions of the low dielectric constant material and the silicon carbide layer, **in claim 7**.

Uglow differs in failing to teach the etch chemical is selected from the group consisting of CF_4 , CHF_3 , CH_2F_2 , and CH_4 ; introducing a selectivity enhancing chemical into the flow of the etch chemical to create a combination flow of the etch chemical and the selectively enhancing chemical, the selectivity enhancing chemical selected from the group consisting of H_2 and NH_3 , the selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material; and the combination flow without substantially removing the exposed low dielectric constant material, **in claim 6**;

introducing a selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into contact with the exposed portions of the silicon carbide layer and the low dielectric constant material, **in claim 9**; and

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into contact with the low dielectric constant material, **as in claim 10**.

Swanson teaches, "Methods for removing SiC are known in the art. The following are some exemplary methods for removing portion 118 of SiC masking layer 104 . . . [. . . Removal rate for SiC relative to SiO_2 of 10:1 has been achieved.] using a chamber pressure: about 300 mTorr (gas flow 10-50 sccm) and RF Power density

Art Unit: 1765

about 0.5-1 W/cm² (13.56 MHz); (2) CF₄ /O₂ /H₂," (column 4, lines 25-43). The aforementioned reads on,

introducing a selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into contact with the exposed portions of the silicon carbide layer and the low dielectric constant material, **in claim 9**; and

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into contact with the low dielectric constant material, **as in claim 10**. and

the etch chemical selected from the group consisting of CF₄, CHF₃, CH₂F₂, and CH₄; and the selectivity enhancing chemical selected from the group consisting of H₂ and NH₃, **in claim 6**. Since Swanson teaches etching the same layers with the same etchants as those of the claimed invention, then using Swanson's etchant in the same manner as that of the claimed invention would result the same in introducing a selectivity enhancing chemical into the flow of the etch chemical to create a combination flow of the etch chemical and the selectively enhancing chemical, the selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material; and the combination flow without substantially eroding the exposed portion of the low dielectric constant material, as in the claimed invention.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Uglow by using a well known method of removing silicon carbide layer as taught by Swanson for the

Art Unit: 1765

purpose of achieving the best selectivity of silicon carbide with respect to a low dielectric constant material with a reasonable expectation of success.

10. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow (US '770 B1) in view of Swanson (US '590) as applied to claim 6 above, and further in view of Conboy et al. (US 5,904,487) and Bhardwaj et al. (US 6,0541,503).

Uglow in view of Swanson differ in failing to specify the selectivity enhancing chemical in a C:H:F ratio of about 1:1:2 to about 1:8:4, **in claim 8** and a temperature range of about -30 to about 80°C, and a power level in a range of about 200 to about 1500 watts, **in claim 11**.

Conboy teaches "Etch rate across the wafer can vary with variation of one or more process parameter including . . . process parameters associated with the plasma including pressure, temperature, composition, flow rate, etc. . . and process parameters associated with the wafer such as temperature" (column 2, lines 12-17) and Bhardwaj teaches the following parameters: . . . chamber pressure, plasma power . . . vary with time (Abstract). Hence, Conboy and Bhardwaj provide evidence that variation in plasma composition (etchant ratio), substrate temperature, chamber pressure and plasma power are so-called "result effective variables."

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Uglow in view of Swanson by varying the plasma composition, pressure, and power and substrate temperature as taught by Conboy and Bhardwaj since it has been held that discovering

Art Unit: 1765

an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 717 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

11. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 1765

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703-305-2667. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

ltue

October 10, 2003

NADINE G. NORTON
PRIMARY EXAMINER

